### End-to-end Real-time Guarantees in Wireless Cyber-physical Systems



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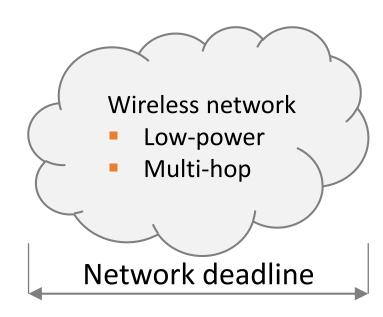


# Predictability is key!

### A Cyber-physical System goes beyond a real-time wireless network

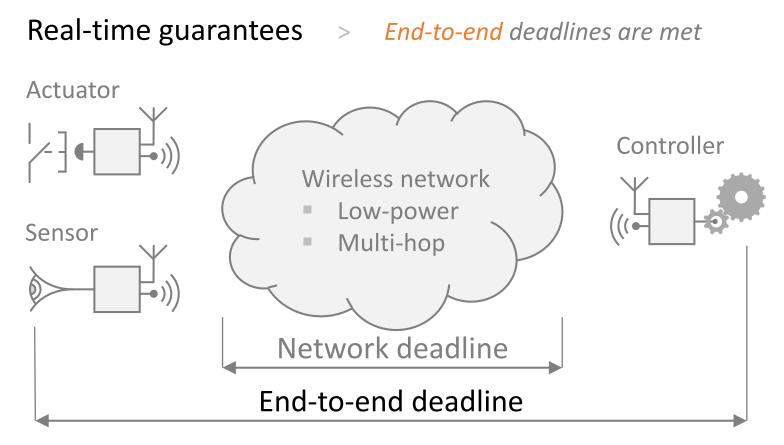
Predictability

Real-time guarantees > Deadlines are met



### A Cyber-physical System goes beyond a real-time wireless network

Predictability



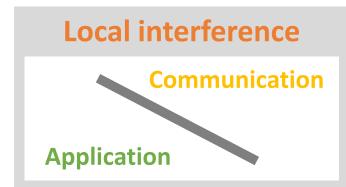
#### A Cyber-physical System goes beyond a real-time wireless network

Predictability

Real-time guarantees Buffer management > No buffer overflow

- End-to-end deadlines are met >

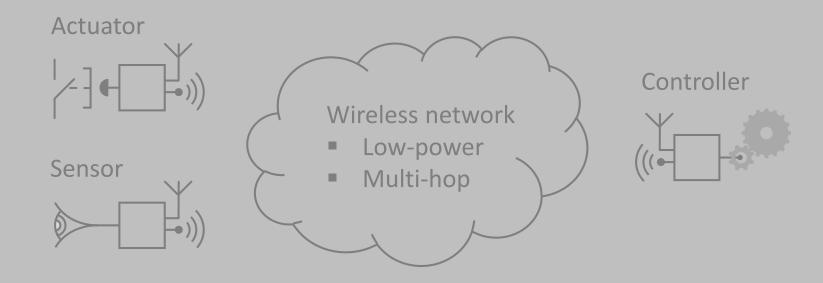




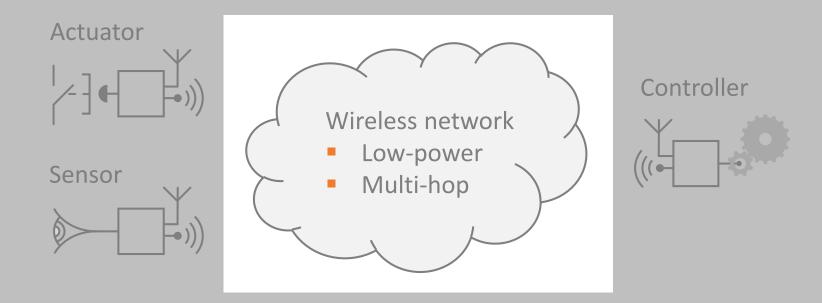
#### Design goals

Predicatability	Network	Device	System
Real-time guarantees			
Buffer management			- 1
Adaptability			- 1
Efficiency			- 1
Composability			

# FirstA predictable and adaptivepiecewireless network



# FirstA predictable and adaptivepiecewireless network



State-of-the-art wireless protocols are *predictable* or *adaptive* 

Splash, RAP

Efficient Adaptive > not Predictable

WirelessHART

Predictable Efficient > not Adaptive BlinkA real-time, reliable and[1]adaptive wireless protocol

Adaptive	Based on Glossy > Flooding primitive
Reliable	<ul> <li>Average 99.97% reception rate</li> <li>Multiple testbeds</li> <li>Tested up to 94 nodes</li> </ul>
Real-time	Online scheduling <ul> <li>EDF-based Lazy Scheduling</li> </ul>

[1] Zimmerling M. et al., *Adaptive Real-time Communication for Wireless Cyber-physical Systems* To appear in ACM Transactions on Cyber-Physical Systems, **2016**  BlinkA real-time, reliable and[1]adaptive wireless protocol

Abstraction

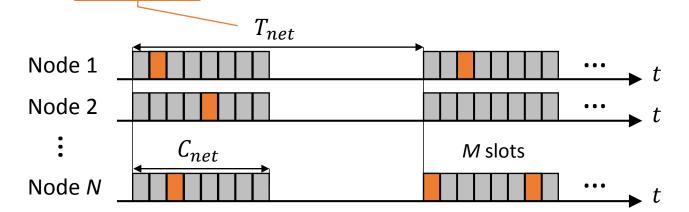
Low-power Wireless Bus (LWB)
> MAC protocol

Communication in rounds

Variable!

#### TDMA-based

Sleep between roundsWireless yields sync!



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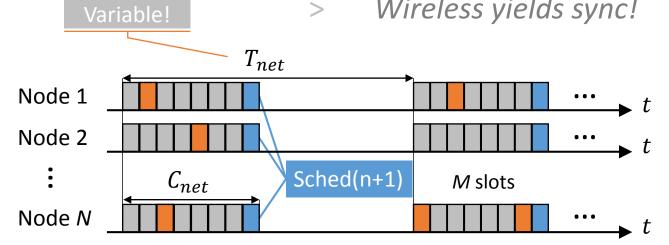
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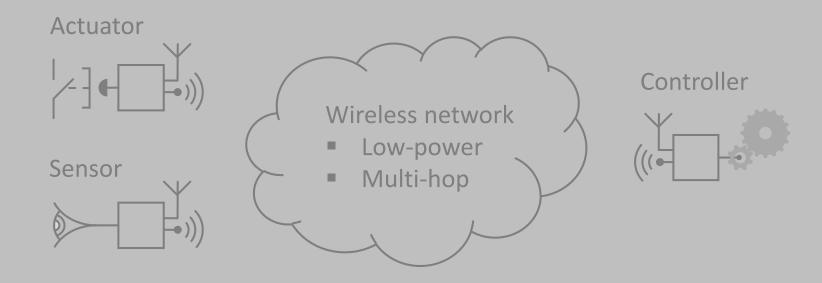


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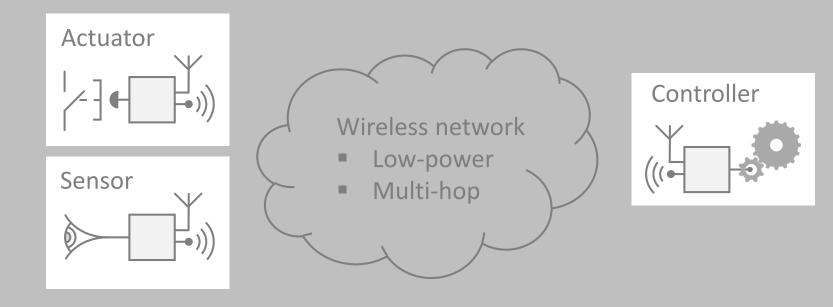
#### Design goals

	Blink		
	Network	Device	System
Real-time guarantees	✓		
Buffer management	na		
Adaptability	$\checkmark$		
Efficiency	$\checkmark$		
Composability	na		

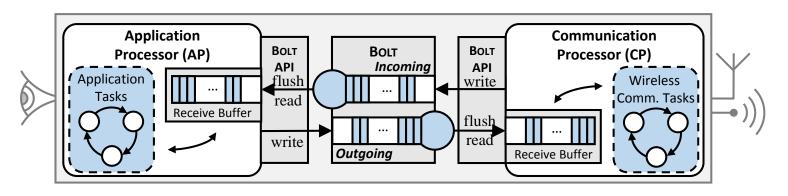
#### Second A *dual-processor architecture* piece to mitigate local interference



#### Second A *dual-processor architecture* piece to mitigate local interference



BoltA dual-processor architecture[2]to mitigate local interference



Real-time behavior

Efficient

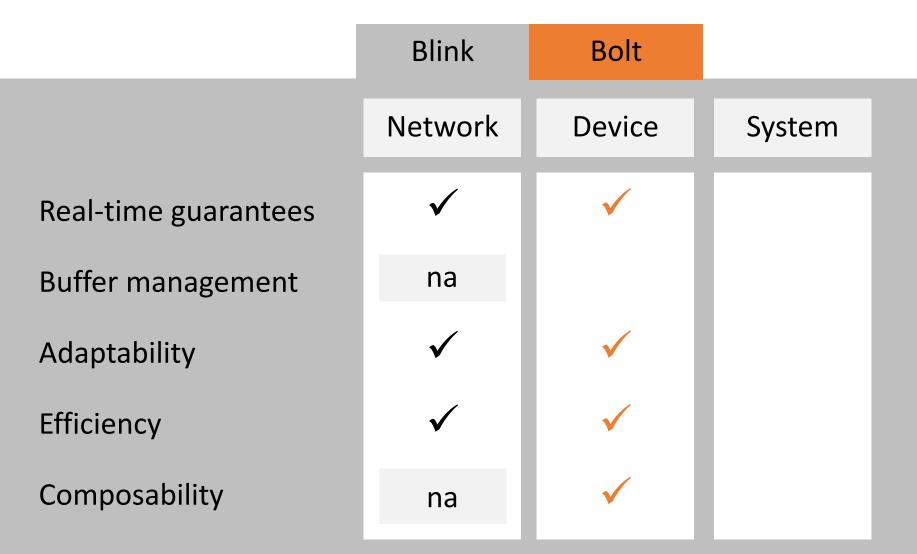
#### Composable

*Formally verified Implemented, tested, deployed* 

μW > sleep mW > active

Hardware/Software *free composition* 

#### Design goals



#### Design goals $\rightarrow$ How can we fill the blanks?

	Blink	Bolt		
	Network	Device	System	
Real-time guarantees	$\checkmark$	$\checkmark$	?	
Buffer management	na	?	?	
Adaptability	$\checkmark$	$\checkmark$	?	
Efficiency	$\checkmark$	$\checkmark$	?	
Composability	na	$\checkmark$	?	

Third Distributed Real-time Protocol (DRP)			
piece	Blink	Bolt	DRP
	Network	Device	System
Real-time guarantees	$\checkmark$	$\checkmark$	?
Buffer management	na	?	?
Adaptability	$\checkmark$	$\checkmark$	?
Efficiency	$\checkmark$	$\checkmark$	?
Composability	na	$\checkmark$	?

DRP is based on three main concepts

Communication is constrained within *registered flows* only

*Global requirements are splited* across distributed components

Interaction between components is based on *contracts* 

#### DRP is based on three main concepts

Communication is constrained within *registered flows* only

*Global requirements are splited* across distributed components

Interaction between components is based on *contracts* 

Communication is constrained within *registered flows* only

Flow *i* 
$$F_i = (n_i^s, n_i^d, T_i, J_i, \mathbf{D}_i)$$

Source Destination Min. release interval Jitter End-to-end deadline

Release model

*Sporatic* with jitter

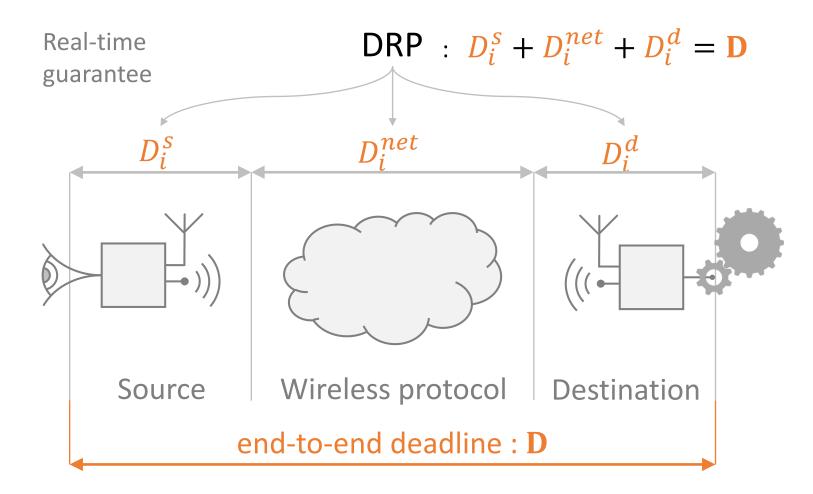
#### DRP is based on three main concepts

Communication is constrained within *registered flows* only

### *Global requirements are splited* across distributed components

Interaction between components is based on *contracts* 

# *Global requirements are splited* across distributed components



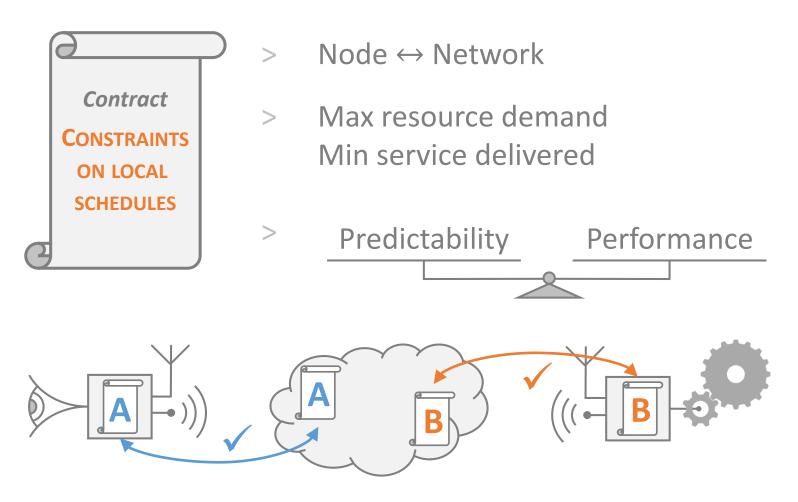
#### DRP is based on three main concepts

Communication is constrained within *registered flows* only

*Global requirements are splited* across distributed components

Interaction between components is based on *contracts* 

## Interaction between components is based on *contracts*

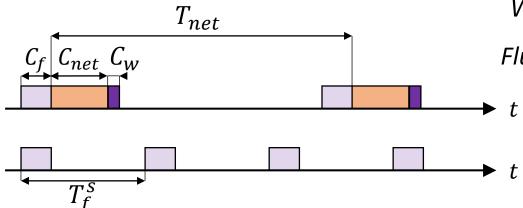


Real-time guarantees Participate in rounds
> T<sub>net</sub> Blink schedule

Flush before rounds Write after rounds > T<sub>net</sub> Blink schedule

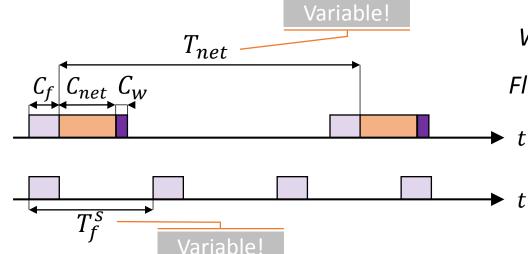
Buffer management Flush Bolt regularly >  $T_f^s$  Comm. Processor schedule

How can we guarantee that all tasks are schedulable?



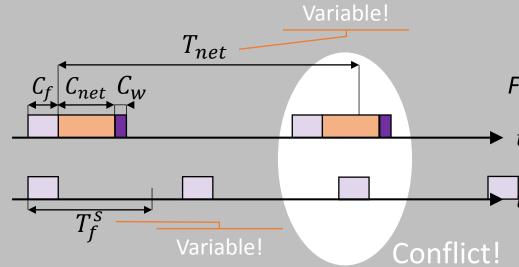
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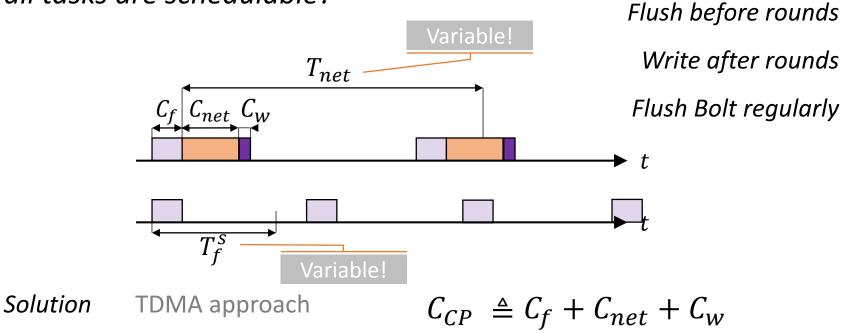
Participate in rounds Flush before rounds Write after rounds Flush Bolt regularly

How to guarantee that all tasks are schedulable?



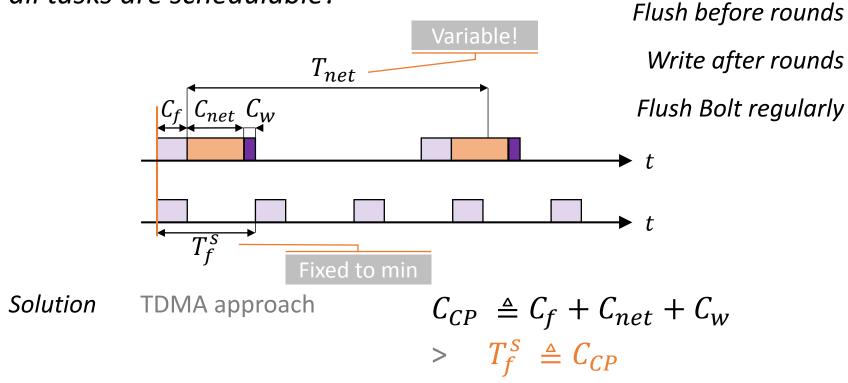
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How to guarantee that all tasks are schedulable?

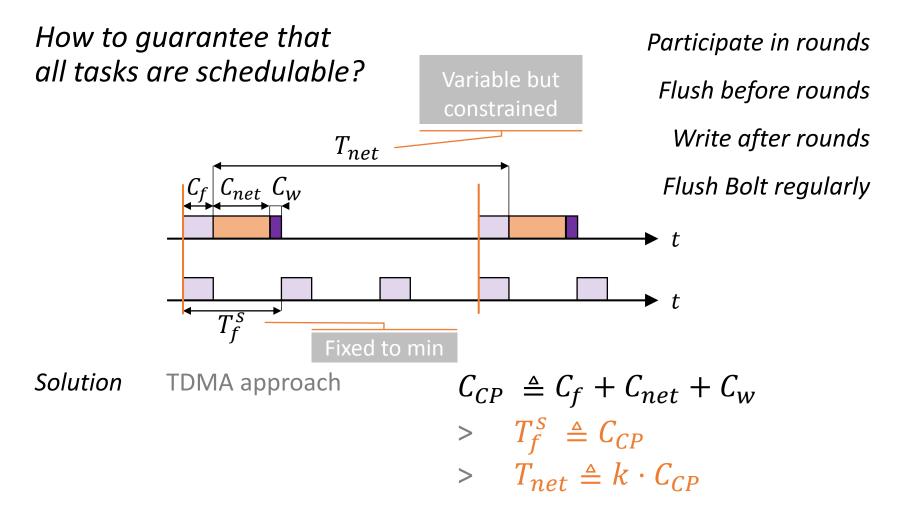


Participate in rounds

How to guarantee that all tasks are schedulable?



Participate in rounds



### Predictability of Network

- + Predictability of Devices
- + DRP contracts
- = System predictability

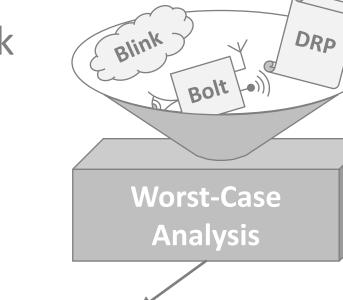
Ultimately

End-to-end latency Buffer size

*Can we set local parameters such that...* 

Flush interval $T_f^S$ Flush interval $T_f^d$ Network deadline $D_i^{net}$ 

If **YES** 



= f(Local parameters)

End-to-end deadlineMemory space

System predictability by design

#### Design goals

	Blink	Bolt	DRP
	Network	Device	System
Real-time guarantees	$\checkmark$	$\checkmark$	?
Buffer management	na	?	?
Adaptability	$\checkmark$	$\checkmark$	?
Efficiency	$\checkmark$	$\checkmark$	?
Composability	na	$\checkmark$	?

#### Design goals

	Blink	Bolt	DRP
Predicatability	Network	Device	System
Real-time guarantees	$\checkmark$	$\checkmark$	✓
Buffer management	na	✓	✓
Adaptability	$\checkmark$	$\checkmark$	?
Efficiency	$\checkmark$	$\checkmark$	?
Composability	na	<ul> <li>✓</li> </ul>	$\rightarrow$

From there, *adaptability* is one (close) step away

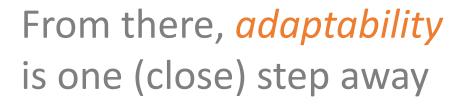
Can we set local parameters such that...

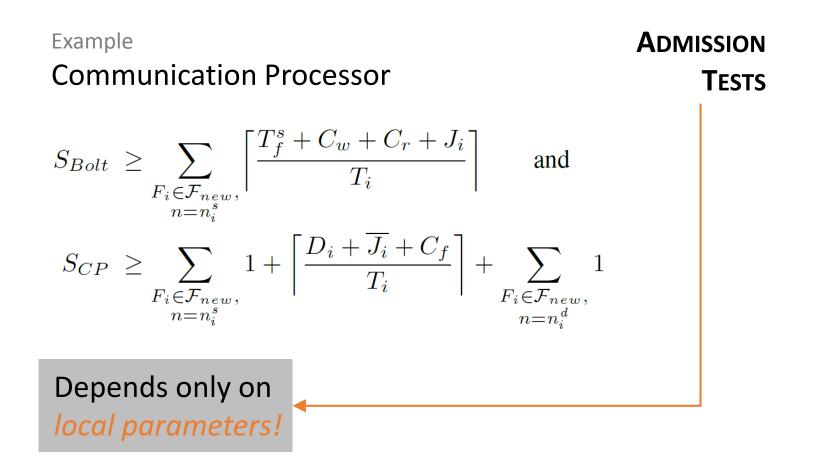
ADMISSION TESTS

End-to-end latency Buffer size

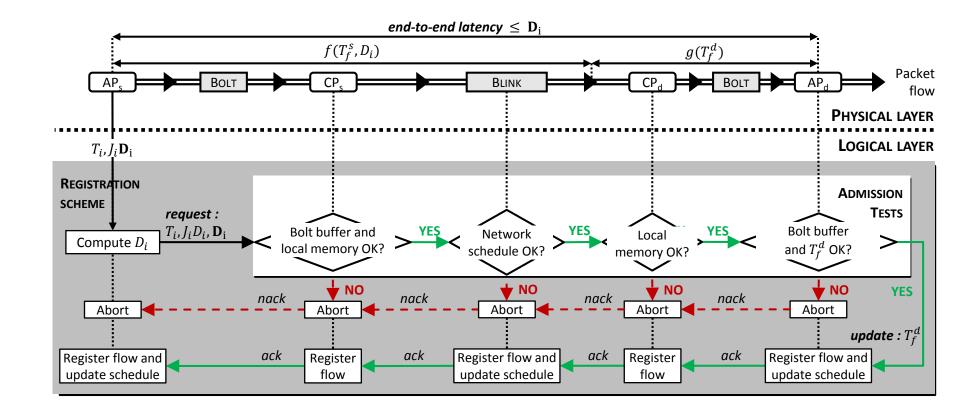
 $\leq$ 

End-to-end deadline Memory space





# Adaptability is achieved via a *distributed registration scheme*

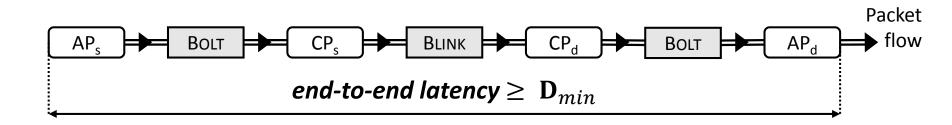


#### Design goals

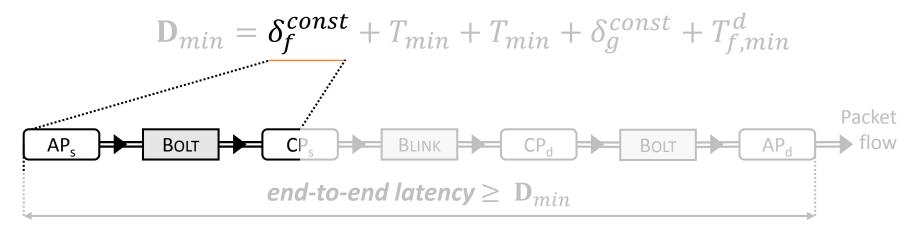
	Blink	Bolt	DRP
Predicatability	Network	Device	System
Real-time guarantees	$\checkmark$	$\checkmark$	$\checkmark$
Buffer management	na	$\checkmark$	$\checkmark$
Adaptability	$\checkmark$	$\checkmark$	✓
Efficiency	$\checkmark$	$\checkmark$	?
Composability	na	$\checkmark$	$\checkmark$

Minimal admissible end-to-end deadline

$$\mathbf{D}_{min} = \delta_f^{const} + T_{min} + T_{min} + \delta_g^{const} + T_{f,min}^d$$



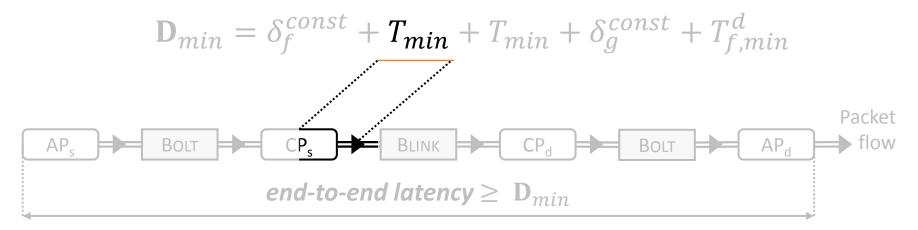
Minimal admissible end-to-end deadline



#### Source delay

- > Message release by the source
- > Available for communication

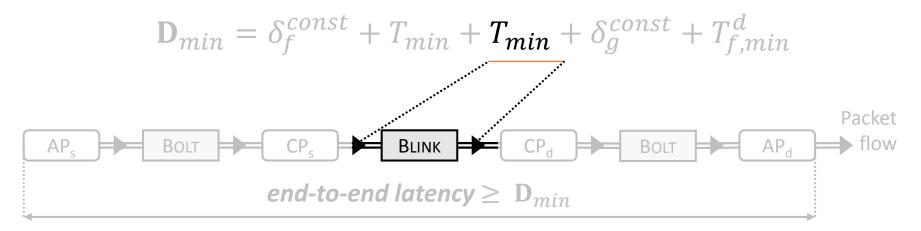
Minimal admissible end-to-end deadline



#### Network delay: Waiting time

- > Message available
- > Message processed by the network

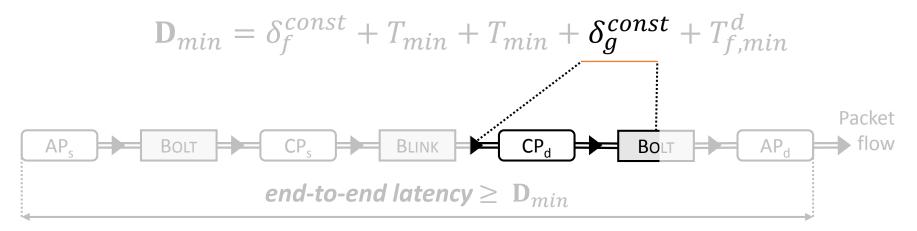
Minimal admissible end-to-end deadline



#### Network delay: Transmission

- > Message processed by the network
- > Message transmitted to the destination node

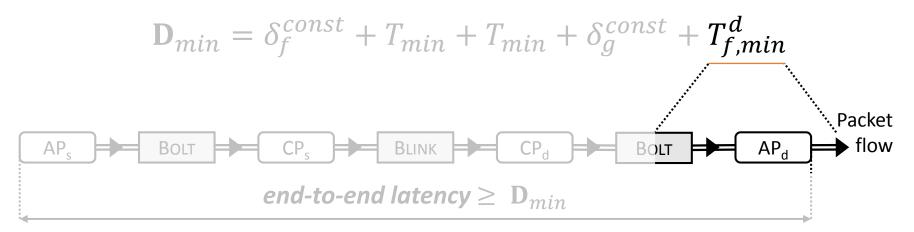
Minimal admissible end-to-end deadline



#### Destination delay: Bolt

- > Message transmitted to the destination node
- > Message available in the Bolt queue

Minimal admissible end-to-end deadline



#### Destination delay: Application

- > Message available in the Bolt queue
- > Message retrieved by the destination application

Minimal admissible end-to-end deadline

$$\mathbf{D}_{min} = \delta_f^{const} + T_{min} + T_{min} + \delta_g^{const} + T_{f,min}^d$$

GivenPacket size32Bytes $C_{net}$ 1s $T_{f,min}^d$ 0.1s

**D**<sub>min</sub> Max data rate

>

3.46 *s* 29.7 *Bps* per flow

#### Design goals

	Blink	Bolt	DRP
Predicatability	Network	Device	System
Real-time guarantees	$\checkmark$	$\checkmark$	$\checkmark$
Buffer management	na	$\checkmark$	$\checkmark$
Adaptability	$\checkmark$	$\checkmark$	$\checkmark$
Efficiency	$\checkmark$	$\checkmark$	✓
Composability	na	$\checkmark$	$\checkmark$

Using *flooding primitives* enables the design of both adaptive AND predictable Wireless Cyber-Physical Systems

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Simulation correlates closely with the analysis

Typical simulation trace result

